

ABSTRACT OF THE DISCLOSURE

Management of Test Access Port functions of a plurality of components arranged on a single chip by selectively driving the TAP function of each of the components with respective clocks, whilst the further signals for driving the TAP function are used in a shared mode among the various components. Preferably, associated with the aforesaid clocks is a pull-down function for selectively blanking the respective clocks in conditions of non-use. In a preferred way, the aforesaid dedicated clocks are generated on board the chip.

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